WHAT IS CLAIMED IS:

1. A high dopant concentration diffused resistor, comprising:

a doped tub located over a semiconductor substrate;

a doped resistor region located in the doped tub, the doped resistor region forming a junction within the doped tub; and

first and second terminals each contacting the doped tub and the doped resistor region, wherein the first and second terminals cause the doped tub and doped resistor region to have a zero potential difference at any point across the junction when a voltage is applied to the first and second terminals.

2. The resistor as recited in Claim 1 wherein the doped tub is a tub resistor and the tub resistor and the doped resistor region function as parallel resistors.

3. The resistor as recited in Claim 1 wherein the semiconductor substrate is a p-type substrate and the doped tub is doped with an n-type dopant and the doped resistor region is doped with a p-type dopant.

4. The resistor as recited in Claim 3 wherein a concentration of the n-type dopant is about 1E16 atoms/cm^3 to about

1E17 atoms/cm^3 and a concentration of the p-type dopant is about 1E18 atoms/cm^3 to about 1E19 atoms/cm^3.

5. The resistor as recited in Claim 1 further including first and second ohmic contacts located at points where the first and second terminals contact the doped tub.

6. The resistor as recited in Claim 5 wherein the first and second ohmic contacts are island regions having a higher dopant concentration of the dopant used in the doped tub.

7. The resistor as recited in Claim 1 wherein the semiconductor substrate is grounded.

8. An integrated circuit, comprising:

transistors located on a semiconductor substrate; and

a high dopant concentration diffused resistor located in the semiconductor substrate adjacent at least one of the transistors, the resistor including;

a doped tub located over the semiconductor substrate;

a doped resistor region located in the doped tub, the doped resistor region forming a junction within the doped tub; and

first and second terminals each contacting the doped tub and the doped resistor region, wherein the first and second terminals cause the doped tub and doped resistor region to have a zero potential difference at any point across the junction when a voltage is applied to the first and second terminals.

9. The integrated circuit as recited in Claim 8 wherein the doped tub is a tub resistor and the tub resistor and the doped resistor region function as parallel resistors.

10. The integrated circuit as recited in Claim 8 wherein the semiconductor substrate is a p-type substrate and the doped tub is doped with an n-type dopant and the doped resistor region is doped with a p-type dopant.

11. The integrated circuit as recited in Claim 10 wherein the at least one of the transistors is formed over an n-typed doped tub and the doped resistor region is doped substantially the same as source and drain regions of the at least one of the transistors.

12. The integrated circuit as recited in Claim 8 further including an interconnect structure located within a dielectric layer overlying the transistors that interconnects the at least one of the transistors and the resistor to form an operative integrated circuit.

13. The integrated circuit as recited in Claim 8 further including first and second ohmic contacts located at points where the first and second terminals contact the doped tub.

14. The integrated circuit as recited in Claim 13 wherein the first and second ohmic contacts are island regions having a higher dopant concentration of the dopant used in the doped tub.

15. The integrated circuit as recited in Claim 8 wherein the semiconductor substrate is grounded.

16. A method of manufacturing a high dopant concentration diffused resistor, comprising:

forming a doped tub over a semiconductor substrate;

forming a doped resistor region in the doped tub, the doped resistor region forming a junction within the doped tub; and

forming first and second terminals each contacting the doped tub and the doped resistor region, wherein the first and second terminals cause the doped tub and doped resistor region to have a zero potential difference at any point across the junction when a voltage is applied to the first and second terminals.

17. The method as recited in Claim 16 wherein forming the doped tub includes forming a tub resistor, and the tub resistor and the doped resistor region function as parallel resistors.

18. The method as recited in Claim 16 wherein the semiconductor substrate is a p-type substrate and forming the doped tub includes doping the doped tub with an n-type dopant and forming the doped resistor region includes doping the doped resistor region with a p-type dopant.

19. The method as recited in Claim 18 wherein doping the doped tub with an n-type dopant includes doping the doped tub to a concentration ranging from about 1E16 atoms/cm^3 to about 1E17

atoms/cm^3, and doping the doped resistor region with a p-type dopant includes doping the doped resistor region to a concentration ranging from about 1E18 atoms/cm^3 to about 1E19 atoms/cm^3.

20. The method as recited in Claim 16 further including forming at least one transistor adjacent the resistor, and connecting the at least one transistor and the resistor to form an operative integrated circuit.

21. The method as recited in Claim 20 wherein forming at least one transistor includes forming source and drain regions simultaneously with the doped resistor region.

22. A high dopant concentration diffused resistor, comprising:

a doped tub located over a semiconductor substrate and doped with a first dopant;

a doped resistor region located in the doped tub and having a higher concentration of the first dopant; and

a first terminal contacting the doped resistor region at a first location and an opposing second terminal contacting the doped resistor region at a second location, wherein the similar dopant between the doped tub and doped resistor region cause them to have a zero potential difference at any point across a junction therebetween when a voltage is applied to the first and second terminals.

23. The resistor as recited in Claim 22 wherein the doped tub is a tub resistor and the tub resistor and the doped resistor region function as parallel resistors.

24. The resistor as recited in Claim 22 wherein the semiconductor substrate is a p-type substrate and the first dopant is an n-type dopant.

25. The resistor as recited in Claim 22 wherein the concentration ranges from about 1E16 atoms/cm^3 to about 1E17

atoms/cm^3 and the higher concentration ranges from about 1E18 atoms/cm^3 to about 1E19 atoms/cm^3.

26. The resistor as recited in Claim 22 wherein the semiconductor substrate is grounded.

27. An integrated circuit, comprising:

transistors located on a semiconductor substrate; and

a high dopant concentration diffused resistor located in the semiconductor substrate adjacent at least one of the transistors, the resistor including;

a doped tub located over the semiconductor substrate and having a concentration of a first dopant;

a doped resistor region located in the doped tub and having a higher concentration of the first dopant; and

a first terminal contacting the doped resistor region at a first location and an opposing second terminal contacting the doped resistor region at a second location, wherein the similar dopant between the doped tub and doped resistor region cause them to have a zero potential difference at any point across a junction therebetween when a voltage is applied to the first and second terminals.

28. The integrated circuit as recited in Claim 27 wherein the doped tub is a tub resistor and the tub resistor and the doped resistor region function as parallel resistors.

29. The integrated circuit as recited in Claim 27 wherein the semiconductor substrate is a p-type substrate and the first dopant is an n-type dopant.

30. The integrated circuit as recited in Claim 29 wherein the at least one of the transistors includes source and drain regions doped substantially the same as the doped resistor region.

31. The integrated circuit as recited in Claim 27 further including an interconnect structure located within a dielectric layer overlying the transistors that interconnects the at least one of the transistors and the resistor to form an operative integrated circuit.

32. A method of manufacturing a high dopant concentration diffused resistor, comprising:

forming a doped tub over a semiconductor substrate and having a concentration of a first dopant;

forming a doped resistor region in the doped tub and having a higher concentration of the first dopant; and

forming a first terminal contacting the doped resistor region at a first location and an opposing second terminal contacting the doped resistor region at a second location, wherein the similar dopant between the doped tub and doped resistor region cause them to have a zero potential difference at any point across a junction therebetween when a voltage is applied to the first and second terminals.

33. The method as recited in Claim 32 wherein forming the doped tub includes forming a tub resistor, and the tub resistor and the doped resistor region function as parallel resistors.

34. The method as recited in Claim 32 wherein the semiconductor substrate is a p-type substrate and forming the doped tub and the doped resistor region includes doping the doped tub and doped resistor region with an n-type dopant.

35. The method as recited in Claim 34 wherein doping the doped tub with an n-type dopant includes doping the doped tub to a concentration ranging from about 1E16 atoms/cm^3 to about 1E17 atoms/cm^3, and doping the doped resistor region with the n-type dopant includes doping the doped resistor region to a concentration ranging from about 1E18 atoms/cm^3 to about 1E19 atoms/cm^3.

36. The method as recited in Claim 32 further including forming at least one transistor adjacent the resistor, and connecting the at least one transistor and the resistor to form an operative integrated circuit.

37. The method as recited in Claim 36 wherein forming at least one transistor includes forming source and drain regions simultaneously with forming the doped resistor region.